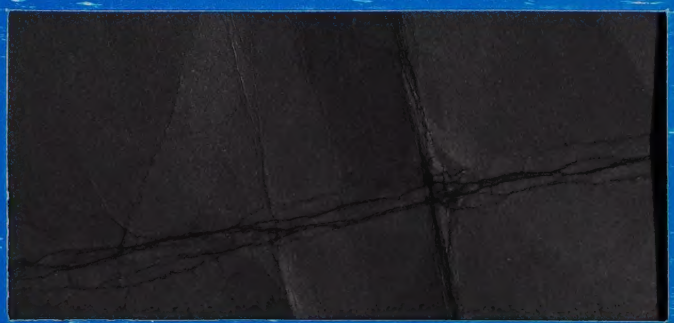
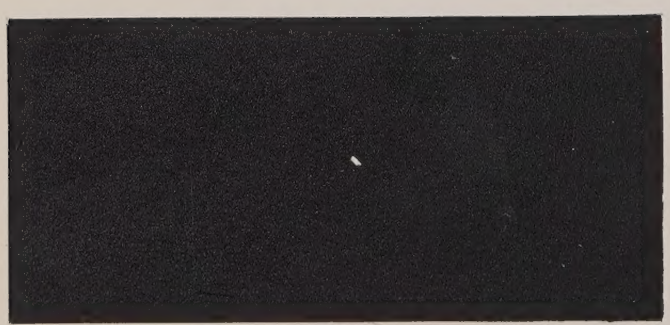
ME-7166 Vol 4 of 5



tau-tron



ME-7166
VOL 4 A5

INSTRUCTION MANUAL

MN-1

PSEUDORANDOM DATA GENERATOR

High-Speed Digital Instrumentation

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MN-1 Pseudorandom Data Generator Front Panel. 4

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INTRODUCTION

Tau-Tron Model MN-1 Pseudorandom Data Generator provides variable length pseudorandom bit patterns for a wide variety of test applications: including communications testing and magnetic tape/disk system testing. Data bit rates from less than 1 Hz to 75 MHz and six pseudorandom code lengths will cover the majority of test situations encountered in the engineering laboratory.

When teamed up with the Tau-Tron Model MB-1 PCM BERT Receiver, a powerful bit error rate measurement system is formed. Bit error rates as low as 1×10^{-10} can be measured. Errors per pseudorandom sequence and cumulative bit error measurements may also be made. The addition of Model MM-1 Data Modifier provides the capability of injecting deliberate bit errors at any desired bit error rate, and the detection of data pattern synchronization at any desired position of the pseudorandom sequence.

For those interested in secure communications problems, data encoder and decoder modes allow the MN-1 to scramble any data input pattern with the selected pseudorandom sequence. Using another MN-1, or the same MN-1 upon playback of magnetic tape/disk, the scrambled data pattern can be decoded to recover the original data input pattern. This technique of scrambling data using pseudorandom bit sequences is in wide use as a means of providing secure communications.

SPECIFICATIONS

All front panel input/output signals are standard TMI levels as defined at the end of this section.

INPUTS

CLOCK IN---From less than 1 Hz to 75 MHz. Minimum pulse width is 5 ns. Input impedance is 50 ohms to ground.

DATA IN---NRZ format data patterns. Input impedance is 50 ohms to ground.

OUTPUTS

CLOCK OUT---Fixed pulse width, 5 ns ± 1 ns.

DATA OUT---NRZ format.

DECODED OUT---Both NRZ and RZ (ERROR) formats. RZ pulse width is 5 ns ± 1 ns.

SYNC OUT---One pulse per selected pseudorandom sequence, in Feedback mode. Pulse width equals one input clock period.

CONTROLS

Mode: FEEDBACK/DECODE/ENCODE---

FEEDBACK - The selected pseudorandom bit sequence appears on the DATA OUT terminal.

DECODE - The input data is divided by the pseudorandom sequence, and the quotient appears on the DECODED OUT terminal.

ENCODE - The input data is multiplied by the pseudorandom sequence, and the product appears on the DECODED OUT and DATA OUT terminals.

TEST---Forces the pseudorandom generator to the all ones state, and a high level appears on the DATA OUT terminal.

CODE LENGTH SELECTION---Six maximum length pseudorandom sequences may be selected. Number of bits per sequence is 2^N-1, where N = 6, 9, 11, 15, 17, or 20.

INDICATORS

CLOCK TRIG'D---LED indicates that proper input clock levels are present: Clock Triggered.

DATA TRIG'D---LED indicates that proper input data levels are present: Data Triggered.

PHASED---LED indicates proper phase alignment of clock and data inputs.

RUN---LED indicates that the pseudorandom sequence generator is operating.

STANDARD TMI SIGNALS

Logical Zero---Between -200 mv and +600 mv.

Logical One---More positive than 1.7 volts.

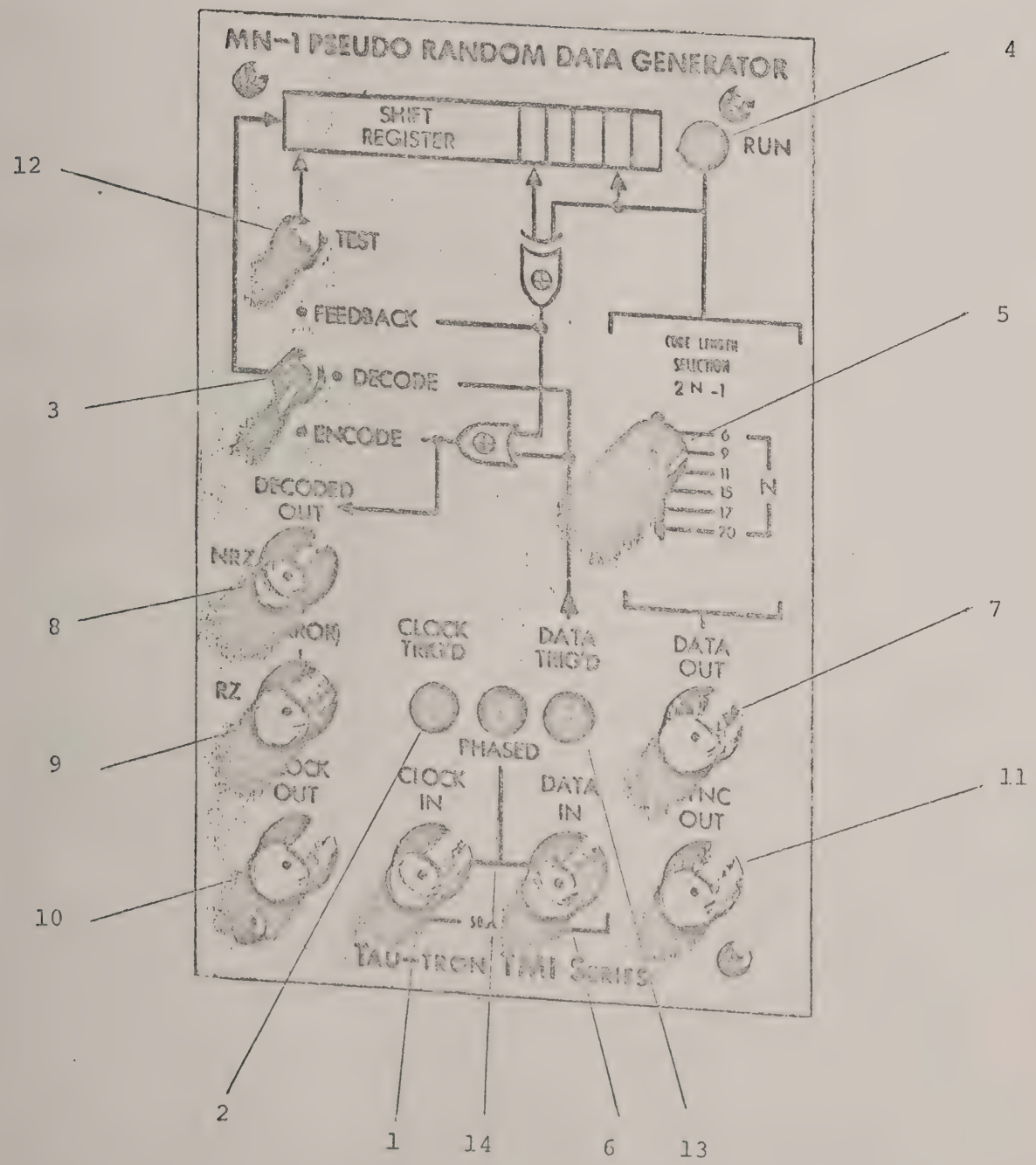
Standard Amplitude---2.0 volts typical.

Transition Edges---Typically 2 ns; 3.5 ns maximum.

Impedance---50 ohms to system ground.

Waveshape Distortion---Less than ±7%, terminated properly.

All outputs must be terminated by 50 ohms to ground for proper signal levels.


MN-1 PSEUDO RANDOM DATA GENERATOR
SHIFT REGISTER
RUN
TEST
FEEDBACK
DECODE
ENCODE
DECODED OUT
CODE LENGTH SELECTION 2 N -1
6
9
11
15
17
20
N
NRZ
RZ
CLOCK TRIG'D
DATA TRIG'D
DATA OUT
PHASED
CLOCK IN
DATA IN
SYNC OUT
TAU-TRON TMI SERIES
1
2
3
4
5
6
7
8
9
10
11
12
13
14

OPERATING INSTRUCTIONS

Model MN-1 Pseudorandom Data Generator provides choice of six pseudorandom sequence lengths over a wide range of operating frequency: from less than 1 Hz to 75 MHz. In addition to use as a data generator, MN-1 can be used to scramble/unscramble data patterns and as a bit error detector. In the following description of these operations, the numbers in parentheses correspond to numbers on the front panel illustration.

DATA GENERATOR

When used as a data generator, only one input is required: the CLOCK IN (1). Standard TMI levels should be used (as described in the Specifications section), and the CLOCK TRIG'D (2) LED will indicate that sufficient levels have been applied to clock the internal logic.

In this mode of operation, the mode switch (3) should be placed in the FEEDBACK position. This connects the feedback exclusive-or function to the input of the shift register as shown on the front panel diagram. At power turn-on, or when the mode is switched to FEEDBACK (3), the shift register generator should automatically start operating. Proper shift register operation is indicated when the RUN (4) LED turns on.

Selection of the desired sequence length (5) is made by selecting the number effective stages in the shift register (N). The number of bits in the pseudorandom sequence will be 2^N-1, as given below:

N = 6	Code Length = 63 bits
N = 9	Code Length = 511 bits
N = 11	Code Length = 2047 bits
N = 15	Code Length = 32767 bits
N = 17	Code Length = 131071 bits
N = 20	Code Length = 1048575 bits

As long as no connection is made at DATA IN (6), the selected pseudorandom sequence is available at three outputs: DATA OUT (7), DECODED OUT NRZ (8), and DECODED OUT RZ (9). DATA OUT (7) is the main output in feedback mode. DECODED OUT NRZ (8) and DECODED OUT RZ (9) are the same information in different formats (NRZ and RZ formats), and represent the selected pseudorandom sequence shifted N (corresponding to code length selection N) bits earlier as compared to DATA OUT (7).

Clock (10) and synchronization (11) outputs are provided along with the data. CLOCK OUT (10) is a fixed width pulse at the input clock frequency. SYNC OUT (11) is a pulse occurring once per pseudorandom sequence length. It is one input clock period wide, and occurs when the shift register contains a logic one in the first bit position, and logic zeroes in the other bit positions.

In order to confirm a system interconnection, it is sometimes desireable to interrupt the output momentarily. The TEST (12) push-button forces the shift register to the all ones state. DATA OUTPUT (7) will be forced to a high level. DECODED OUT NRZ (8) will follow the DATA IN (6) level. DECODED OUT RZ (9) will pulse if DATA IN (6) is a high level.

SCRAMBLE/UNSCRAMBLE DATA PATTERNS

In addition to the CLOCK IN (1), a DATA IN (6) is also provided. This can be any desired pattern. As long as both proper signal levels are present, the DATA TRIG'D (13) LED will light. The PHASED (14) indicator will light if the clock and data are properly phase related.

Selecting the ENCODE position of the mode switch (3) will cause the incoming data pattern to be multiplied by the pseudorandom sequenced selected (5). The resulting product will be a scrambled, unpredictable data pattern, and will be available at the DATA OUT (7), the DECODED OUT NRZ (8) , and the DECODED OUT RZ (9). The two decoded out (8 and 9) signals are shifted N (5) bits in time (earlier) as compared to the DATA OUT (7).

Scrambled data may then be applied to the user's system. When the scrambled data is recovered from the user's system, it can be decoded by another MN-1. If the user's system is a magnetic tape, disk, or other data storage device, it is possible to playback the recorded scrambled data pattern into the same MN-1.

DECODE mode is selected by the mode switch (3), and clock/data inputs are applied to the MN-1 as before. In this case the input data pattern is divided by the selected pseudorandom sequence (5), and the resulting quotient will be the original data pattern (applied to the MN-1 in ENCODE mode). The quotient is available at the DECODED OUT NRZ (8) and DECODED OUT RZ (9) terminals. DATA OUT (7) will be the incoming scrambled pattern shifted N (5) times.

CLOCK OUT (10) is available in this mode as in FEEDBACK mode. SYNC OUT (11), however, will be indeterminate. It will be a high level for one clock period whenever a logic one is detected in shift register position one, with logic zeroes in all other shift register positions.

BIT ERROR DETECTOR

While the Tau-Tron Model MB-1 is a much more powerful BERT receiver, combining bit error detection with error rate measurement; it is possible to operate the MN-1 generator as a bit error detector. The resulting RZ error signal can then be used to drive an external counter.

First CLOCK IN (1) and DATA IN (6) must be applied to the MN-1 and properly PHASED (14). Then the user must select the same pseudo-random sequence (5) as he expects at the data input (6).

By placing the MN-1 into DECODE MODE (3), the internal shift register is synchronized with the incoming pattern after N (5) consecutive error-free bits have been received. Switching the mode switch (3) back to FEEDBACK will lock the internal shift register to the proper pseudorandom sequence. It will be present at DATA OUT (7). The

encoder/decoder exclusive-or function is now comparing the internally generated sequence with the input data (6) on a bit-by-bit basis. DECODED OUT NRZ (8) will be true whenever an error bit is detected (for the entire data bit period). DECODED OUT RZ (7) will be a fixed width pulse for each bit error detected, and may be used to drive an external counter to totalize the number of errors detected. (Be sure that the external counter can accept the fixed width error pulse. The pulse may have to be widened for the particular counter used.)

TIMING CONSIDERATIONS

INPUTS

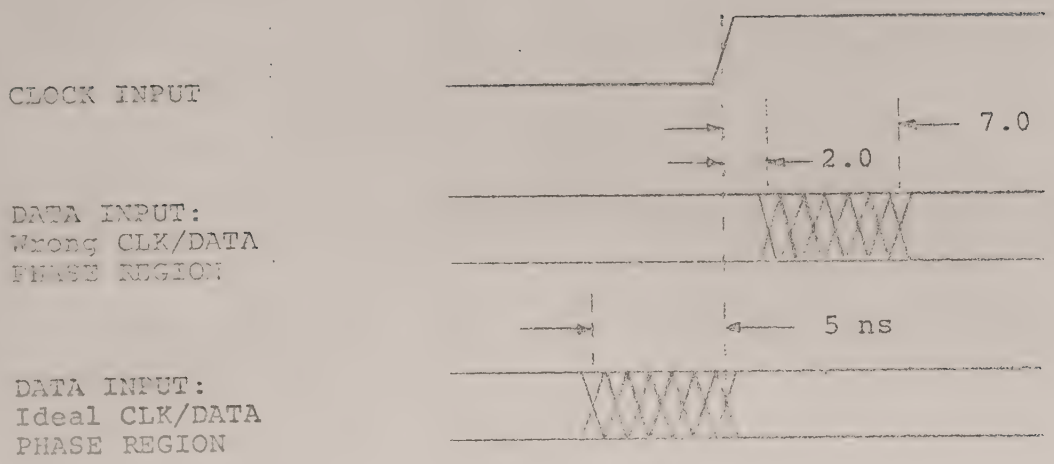
Clock and data must not be edge aligned at the data input latch to prevent ambiguity. Furthermore, setup time at the latch is a minimum of 2.5 ns. Hold time is a minimum of 1.5 ns. Since the internal clock path is typically four ns longer than the internal data path to the data input latch, this translates to the forbidden region show in the Input Timing diagram where the clock edge must not reside in the 5 ns region leading the NRZ data edge.

An ideal phase setting region is clock edge aligned or lagging input data by up to 5 ns. This will assure that set up and hold times are proper at the data input latch over the entire frequency range of the module.

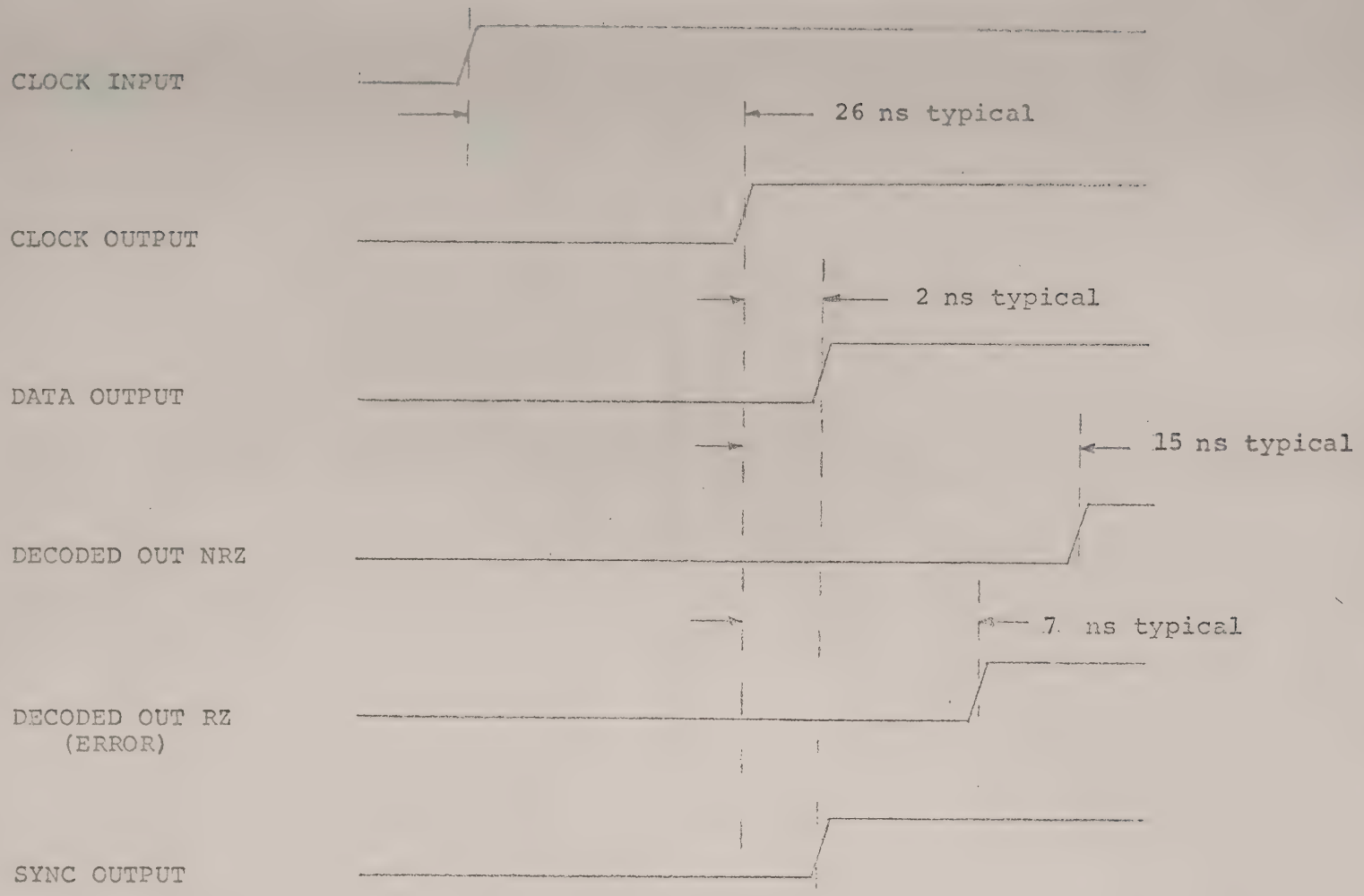
When setting up clock and data initially, simply monitor the TRIG'd LED's and the DECODED OUT NRZ, with the TEST button depressed this output will follow the input data in any of the three modes of operation.

OUTPUTS

The timing relationships of the various output signals are shown on the Output Timing diagram.



INPUT TIMING DIAGRAM



OUTPUT TIMING DIAGRAM

THEORY OF OPERATION

Tau-Tron Model MN-1 Pseudorandom Data Generator produces six different pseudorandom sequences utilizing a variable length shift register with appropriate feedback taps for maximum sequence length. This means that the length of any sequence selected will be a function of the number of stages in the shift register, and will produce all possible shift register states except all zeroes. Sequence length can be calculated by the formula, length = 2^N-1, where N = the number of stages in the shift register. All zeroes is an illegal shift register state because the feedback function will "hang up" at logical zero if the all zeroes state exists.

In addition to feedback operation, the shift register input can be switched to allow encoding and decoding operations.

INPUT CIRCUITS

Clock and data inputs are received by differential type amplifiers and converted to ECL levels. Acceptable input levels are determined by feeding each input to the clock of a toggle-mode flip flop. Each flip-flop output drives a capacitively-coupled LED driver. As transitions are detected in the input waveform, the LED turns on momentarily. At the usual operating frequencies the triggered LED's will be on continuously.

The clock/data phased detector is similar. The data waveform drives the clock input of a D flip flop (D always logic one), while the 5 ns fixed width internal clock drives the reset input. The output of this phase flip flop drives a toggle-mode flip flop and LED driver as described above.

PSEUDORANDOM GENERATOR (FEEDBACK OPERATION)

In the MN-1 maximum codes are produced for shift registers which have 6, 9, 11, 15, 17, and 20 stages (selections 1 through 6 respectively in the lower left corner of the schematic). The taps for these code lengths are listed on the schematic. For reasons of propagation

delay in high speed shift registers, the generator is implemented so that there is never more than two gate delays between register stages, even at the shift register input. This requires that a delta register be used to set up the number of stages between the last stage tap and the mid-stage tap. The mid-stage tap is one fixed input to the exclusive-or circuit, and the gate multiplexer sets up the appropriate number of stages to the fixed last stage flip-flop. Also the appropriate number of stages from the first stage to the mid-stage is set up by a second gate multiplexer. Using this high speed method restricts the lengths of maximum-length PN codes generated to those with only two taps within range of the delta register. Deltas for each PN code length are also shown on the schematic.

Since the all zeroes state is illegal, a zero detector is used to monitor the number of active stages for the code length selected. Should all zeroes be detected at power-on or any other time, the first stage would be forced to logic one. To conserve on logic, the PN sync detector is implemented in the zero detector. A PN sync is generated whenever the shift register contains a logic one in its first stage, and a logic zero in all other stages.

When the TEST pushbutton is depressed on the front panel, a logic one is forced into the first stage of the shift register. After N clock periods, the entire shift register, as well as the data output, will be at the logic one level.

ENCODE/DECODE OPERATION

Via front panel control, the input to the shift register can be switched to three possible sources. If the output of the shift register feedback (exclusive-or) function is selected, FEEDBACK operation results.

The data input is always compared to the shift register feedback function by an exclusive-or gate. If the output of this comparison exclusive-or gate is selected as the shift register input, ENCODE

operation results. In this mode, the incoming data pattern is being multiplied by the pseudorandom sequence.

If the incoming data is selected to be the direct input of the shift register, DECODE operation results. In this mode, the incoming data pattern is being divided by the pseudorandom sequence.

It can be seen that in FEEDBACK operation, the comparison exclusive-or is essentially detecting the differences between the locally generated pseudorandom sequence and the incoming data pattern. By switching to DECODE operation for N clock periods, the local generator will lock onto the incoming pattern (assuming it is a pseudorandom sequence of the same length as the local generator selection; and that the N bits were error-free). When switched back to FEEDBACK operation, the comparison exclusive-or will detect the difference (errors) between the incoming pattern and the locally generated pseudorandom sequence.

OUTPUT CIRCUITS

Complementary output amplifiers are located on a separate PC card within the module. Five signals are brought over from the PR Generator card: output clock, pseudorandom sync, generator data output, and the NRZ and RZ outputs from the comparison exclusive-or. The true signals are brought out to the front panel, while the false signals are internally terminated on the Amplifier PC card.

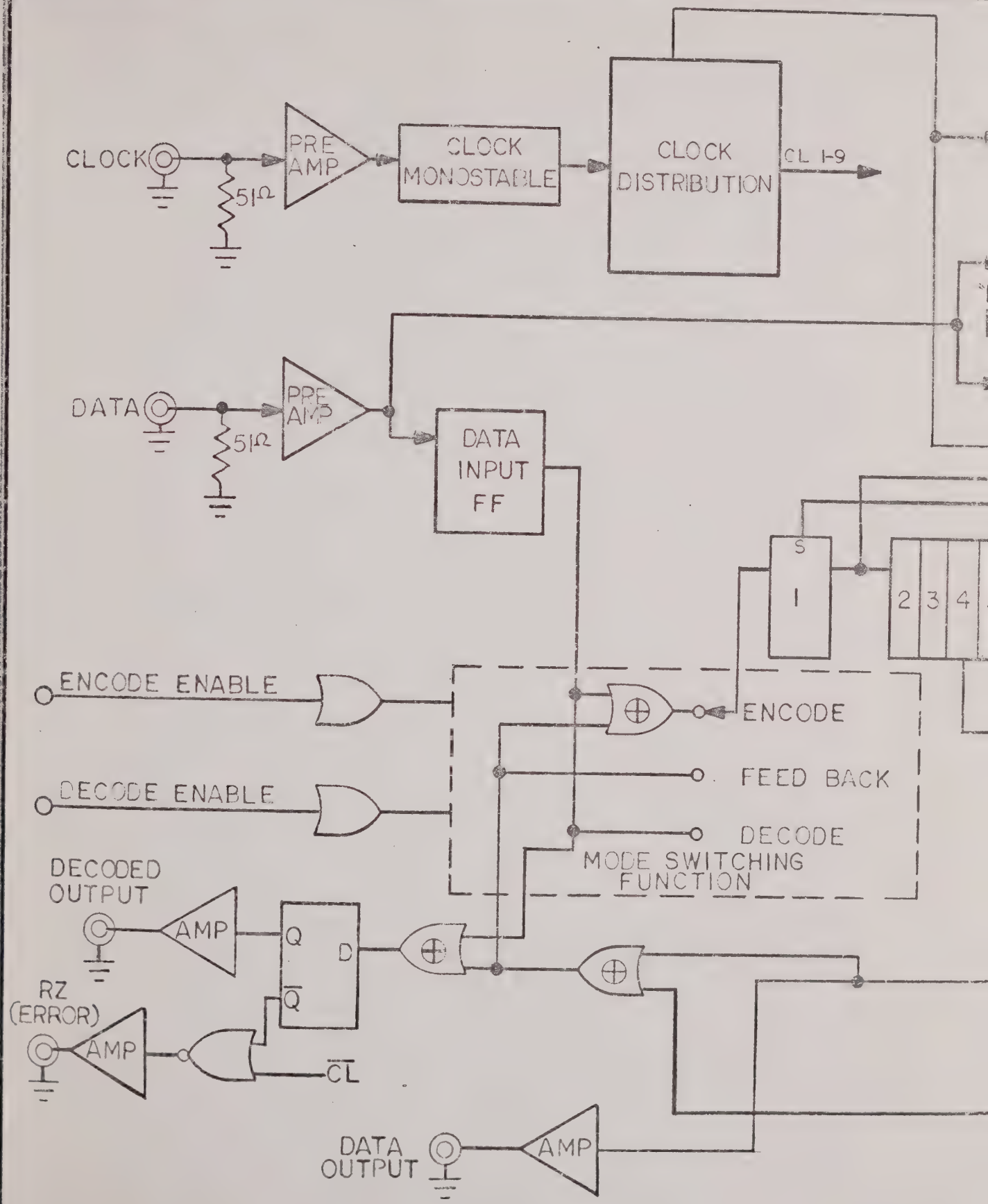
LIST OF ILLUSTRATIONS

MN-1 Block Diagram TBN-53177

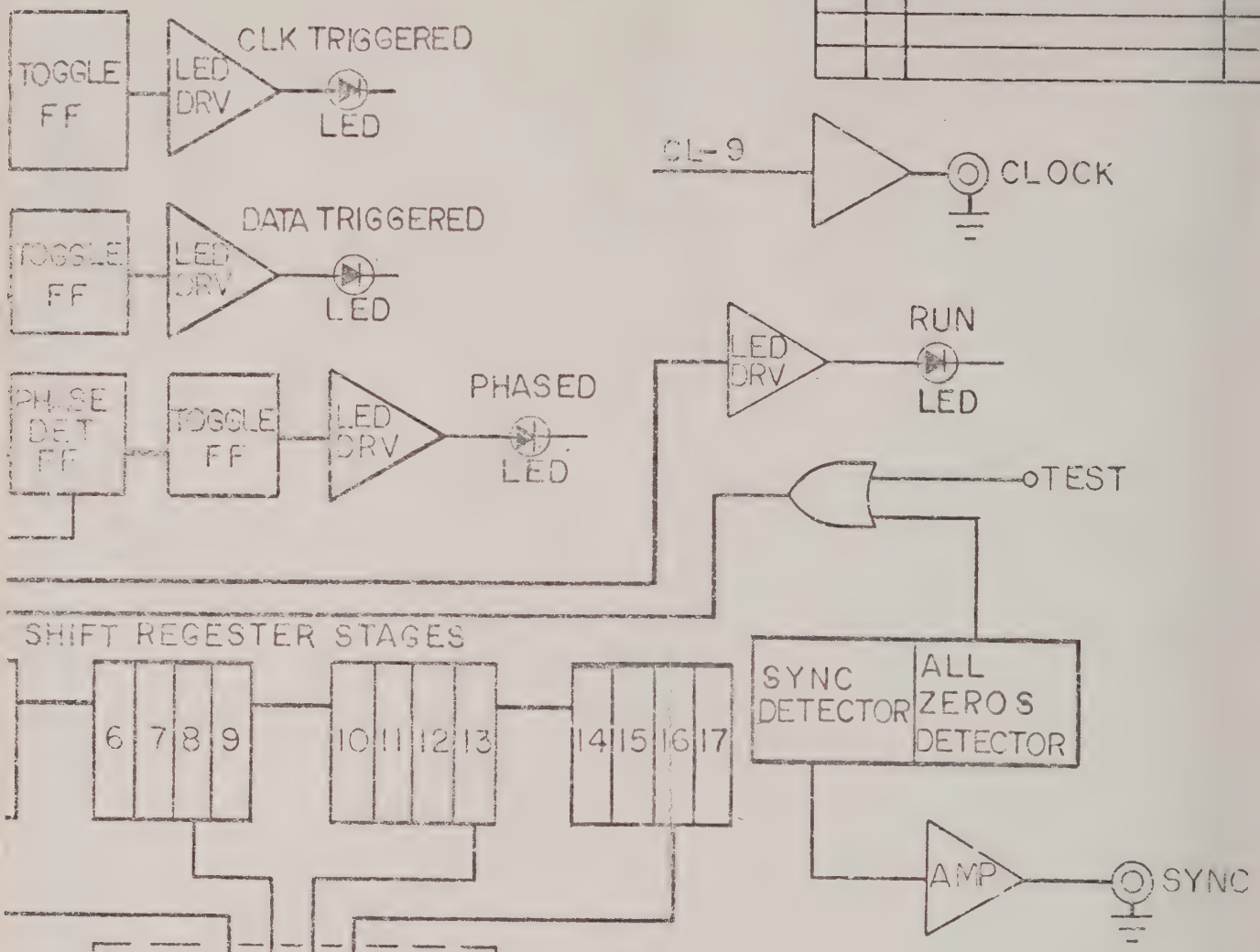
Module Power Supply Schematic. TAJ-53383

MN-1 Pseudorandom Number Generator Schematic TDJ-53234

MN-1 Five Channel Output Amplifier TDJ-53204


CLOCK
51Ω
PRE AMP
CLOCK MONOSTABLE
CLOCK DISTRIBUTION
CL 1-9
DATA
51Ω
PRE AMP
DATA INPUT FF
S
1
2
3
4
ENCODE ENABLE
ENCODE
FEED BACK
DECODE ENABLE
DECODE
MODE SWITCHING FUNCTION
DECODED OUTPUT
AMP
Q
D
Q̄
RZ (ERROR)
AMP
CL̄
DATA OUTPUT
AMP

DATE	SYM	REVISION RECORD	DR.	CK.

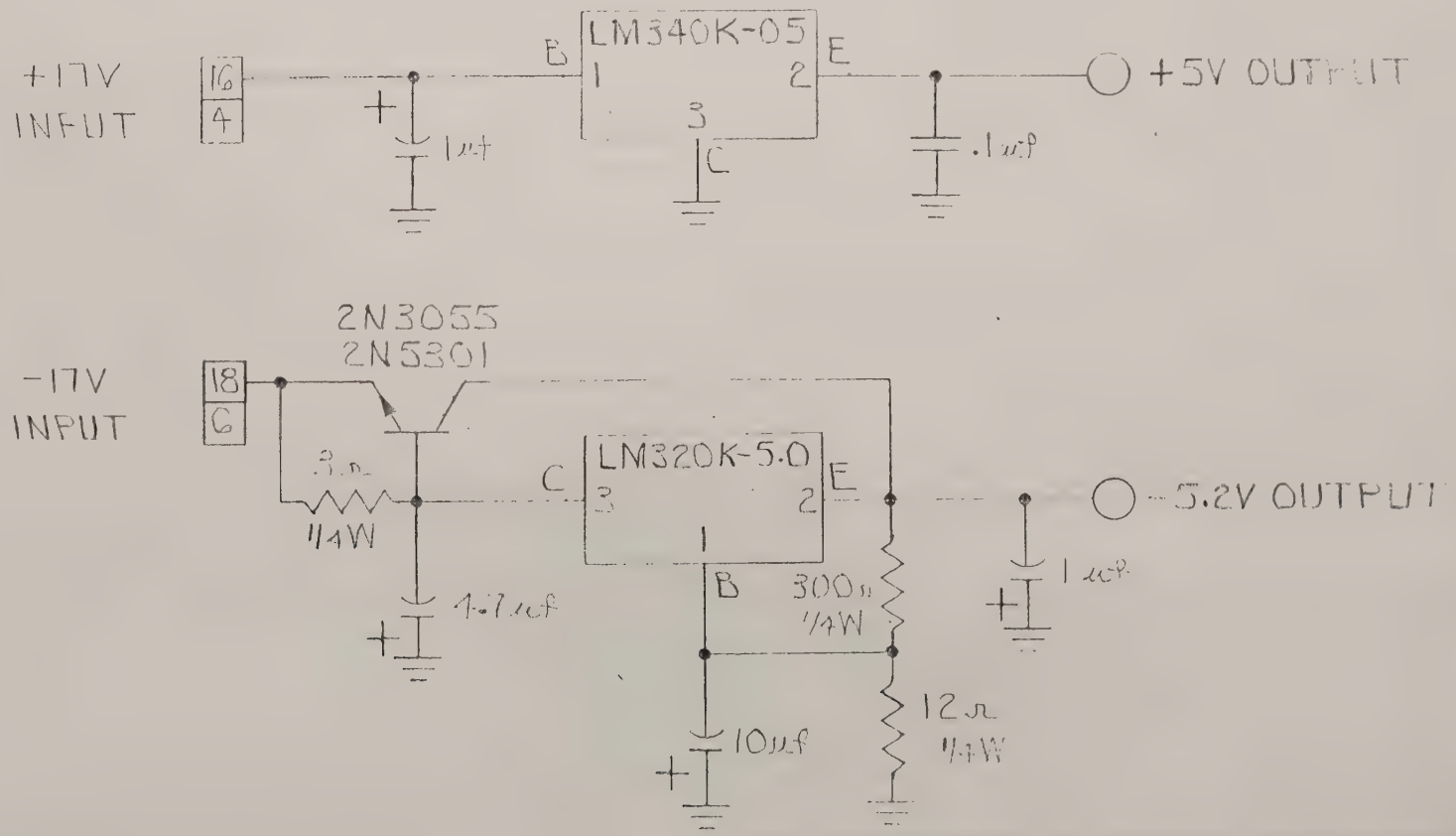


FRONT PANEL TAP SELECTION SWITCH POSITION

		6	9	11	15	17	20
SHIFT REG STAGE	A	5	5	9	14	14	17
	B	C	9	11	15	17	20
TAP SPACING		Δ1	Δ4	Δ2	Δ1	Δ3	Δ3

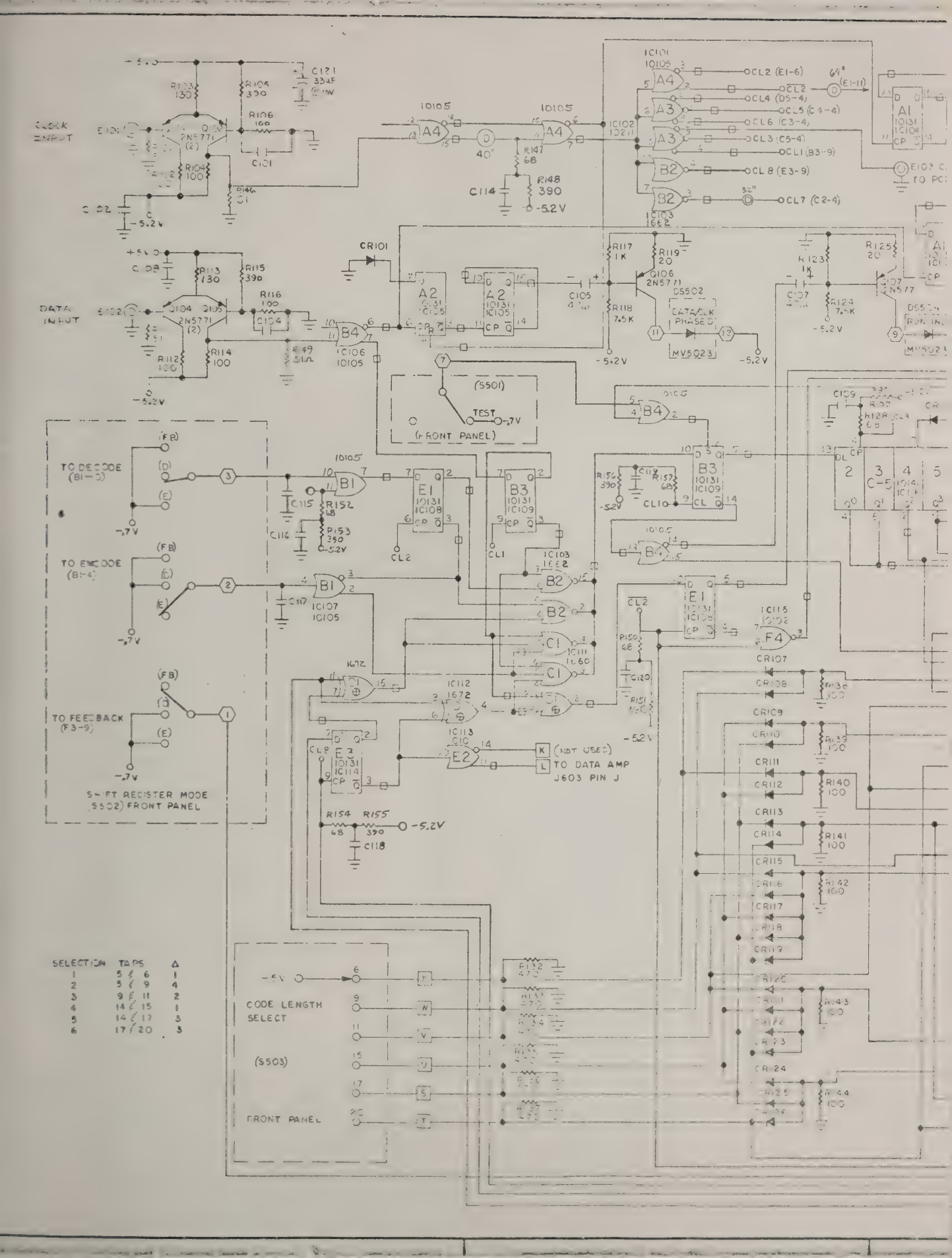
TOLERANCES (EXCEPT AS NOTED)	TAU-TRON, INC		
DECIMAL ± .XX	TMI SERIES	SCALE .XX	DRAWN BY JHB APPROVED BY
FRACTIONAL ± XX	TITLE BLOCK DIAGRAM MN-1		
ANGULAR ± XX	DATE 1-24-72	DRAWING NUMBER TBN 53177	

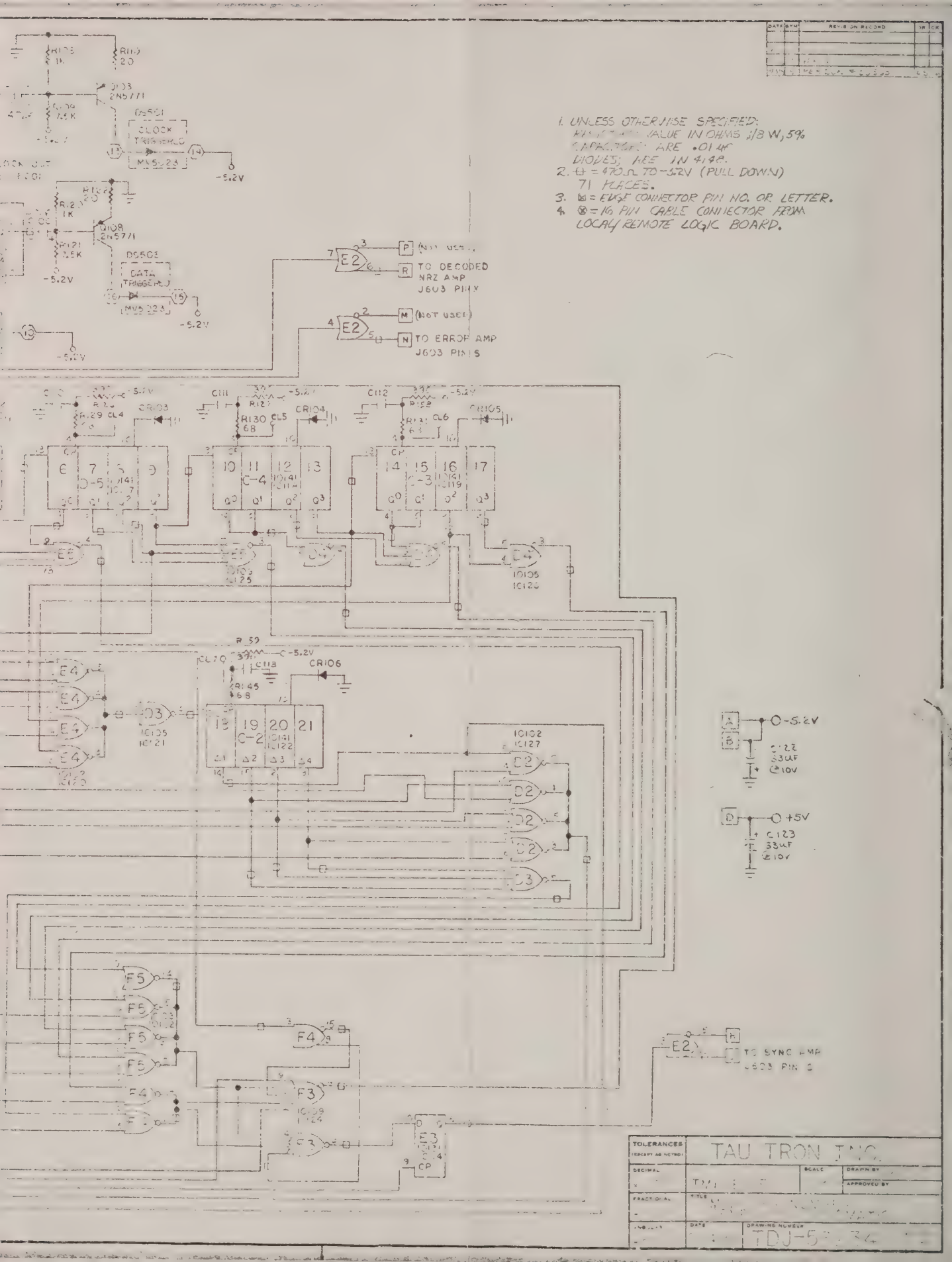
DATE	SYM	REVISION RECORD	DR.	CK.

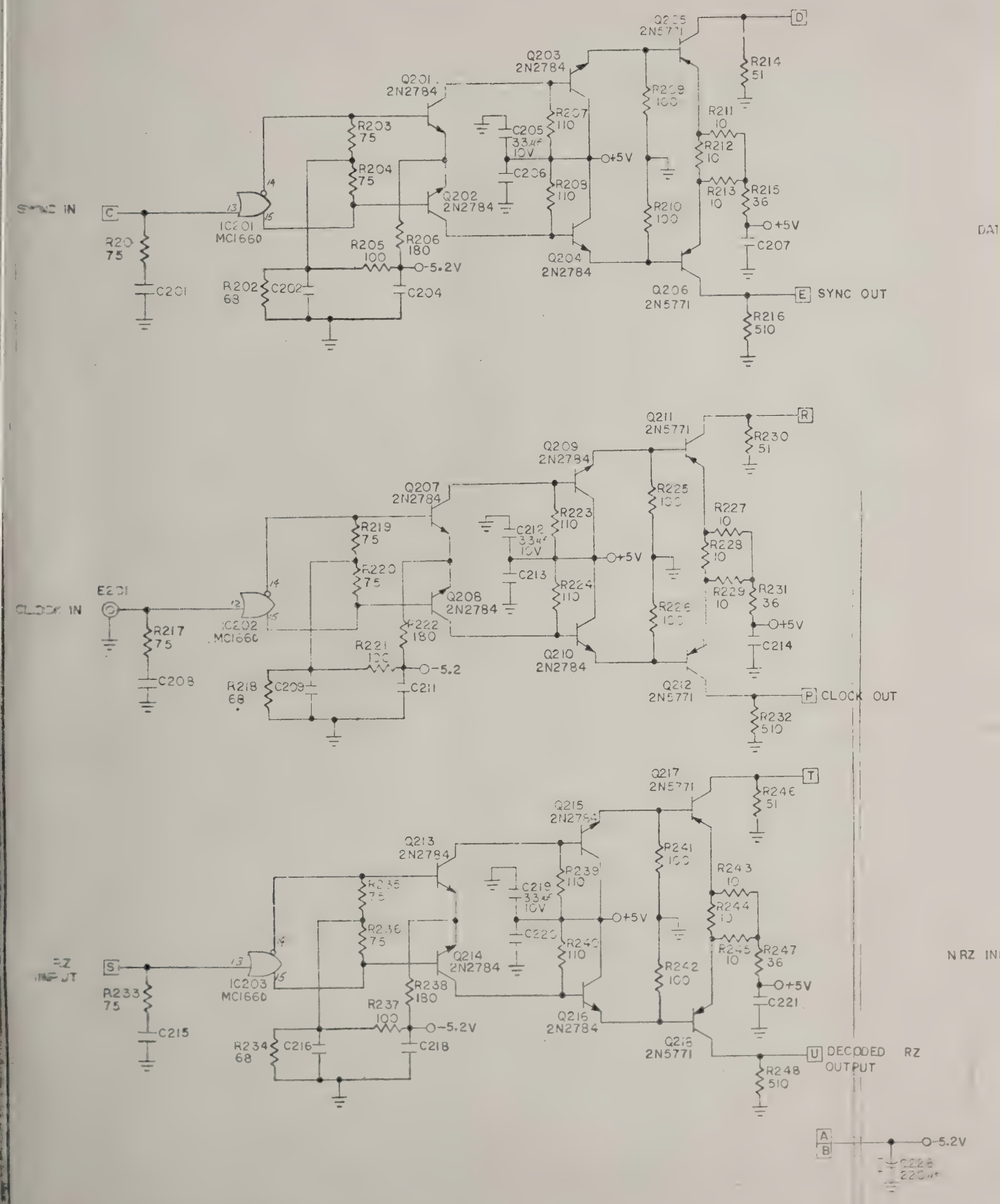


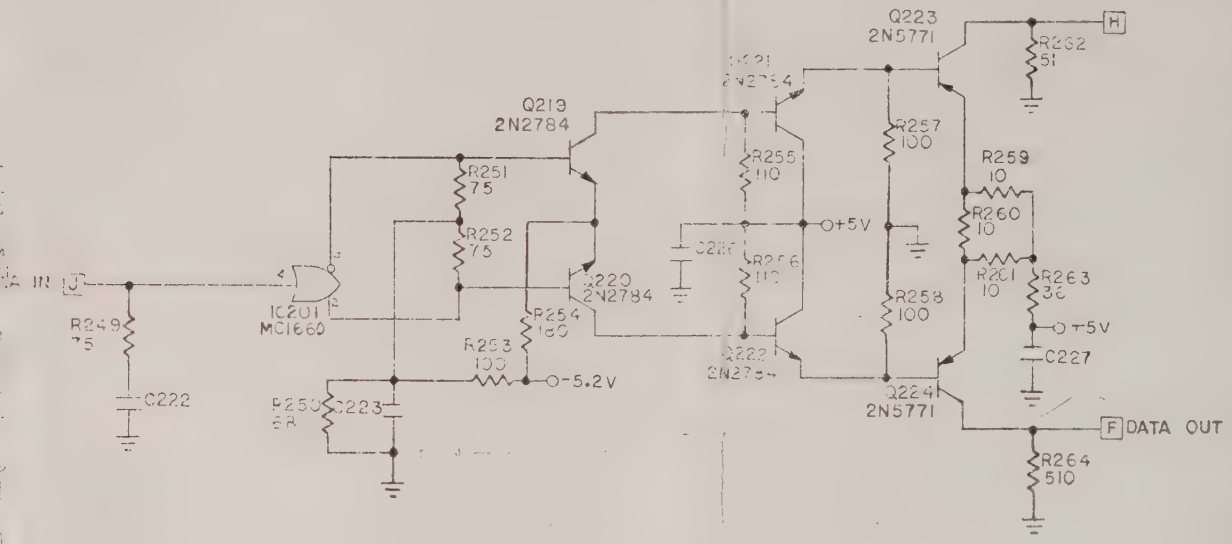
TOLERANCES (EXCEPT AS NOTED)	TAU-TRON INC.		
DECIMAL ±	TMI SERIES	SCALE —	DRAWN BY APPROVED BY
FRACTIONAL ±	TITLE SCHEMATIC MODULE POWER SUPPLY (+5V, -5.2 VOLT)		
ANGULAR ±	DATE 11/5/74	DRAWING NUMBER TAJ-53583	

RUNING 40-21


CLOCK INPUT
DATA INPUT
TO DECODE (B1-3)
TO ENCODE (B1-4)
TO FEEDBACK (F3-9)
SHIFT REGISTER MODE (S502) FRONT PANEL
(S501)
TEST
(FRONT PANEL)
CODE LENGTH SELECT
(S503)
FRONT PANEL
TO DATA AMP J603 PIN J
(NOT USED)
TO PC
SELECTION TAPS Δ
1 5 & 6 1
2 5 & 9 4
3 9 & 11 2
4 14 & 15 1
5 14 & 17 3
6 17 & 20 3

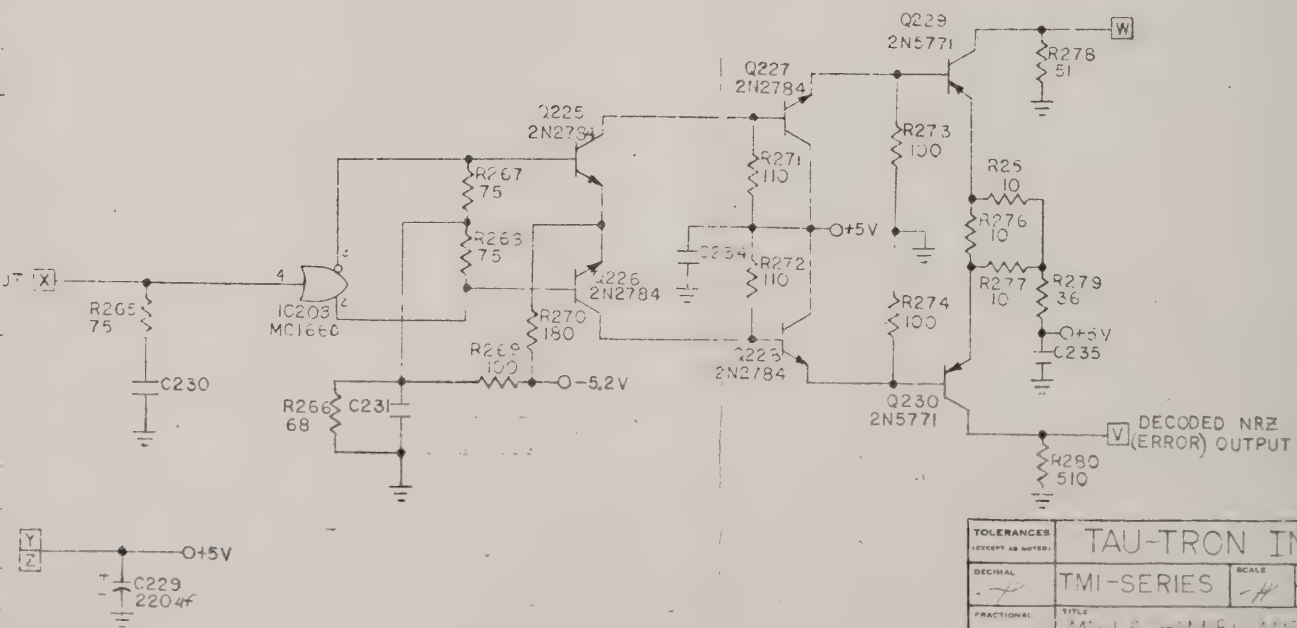

1. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUE IN OHMS 1/8 W, 5%
CAPACITORS ARE .01 μF
DIODES; 1/2 IN 4198.
2. ⊖ = 470Ω TO -5.2V (PULL DOWN)
71 PLACES.
3. ⊠ = EDGE CONNECTOR PIN NO. OR LETTER.
4. ⊗ = 16 PIN CABLE CONNECTOR FROM
LOCAL/REMOTE LOGIC BOARD.
R103 1K
R110 20
Q103 2N5771
R109 7.5K
D0502
CLOCK TRIGGERED
MV5023
-5.2V
R122 20
1K
Q108 2N5771
R121 7.5K
D0503
DATA TRIGGERED
MV5023
E2
P (NOT USED)
R
TO DECODED NRZ AMP J603 PIN X
M (NOT USED)
N
TO ERROR AMP J603 PIN 5
R129 CL4
CR103
C111
R130 CL5 68
CR104
C112
R131 CL6 68
CR105
C-4
C-3
C-2
C-5
10141
10119
10125
10105
10120
R 59
C113
CR106
CL7 0
R145 68
10105
10121
10102
10127
D2
D3
C122 33uF @10V
C123 33uF @10V
+5V
F5
F4
F3
10109
10124
CP
TO SYNC AMP J603 PIN 8
TAU TRON INC.
TOLERANCES
DECIMAL
FRACTIONAL
SCALE
DRAWN BY
APPROVED BY
TITLE
DATE
DRAWING NUMBER
TDJ-5


SYNC IN
C
R201 75
C201
IC201 MC1660
R202 68
C202
R203 75
R204 75
Q201 2N2784
Q202 2N2784
R205 100
-5.2V
R206 180
C204
Q203 2N2784
Q204 2N2784
C205 33uF 10V
C206
+5V
R207 110
R208 110
Q205 2N5771
R209 100
R210 100
R211 10
R212 10
R213 10
R214 51
R215 36
+5V
C207
D
Q206 2N5771
E
SYNC OUT
R216 510
DAT
CLOCK IN
E201
R217 75
C208
IC202 MC1660
R218 68
C209
R219 75
R220 75
Q207 2N2784
Q208 2N2784
R221 100
-5.2
R222 180
C211
Q209 2N2784
Q210 2N2784
C212 33uF 10V
C213
+5V
R223 110
R224 110
Q211 2N5771
R225 100
R226 100
R227 10
R228 10
R229 10
R230 51
R231 36
+5V
C214
R
Q212 2N5771
P
CLOCK OUT
R232 510
RZ INPUT
S
R233 75
C215
IC203 MC1660
R234 68
C216
R235 75
R236 75
Q213 2N2784
Q214 2N2784
R237 100
-5.2V
R238 180
C218
Q215 2N2784
Q216 2N2784
C219 33uF 10V
C220
+5V
R239 110
R240 110
Q217 2N5771
R241 100
R242 100
R243 10
R244 10
R245 10
R246 51
R247 36
+5V
C221
T
Q218 2N5771
U
DECODED RZ OUTPUT
R248 510
NRZ INP
A
B
-5.2V
C228 220uF



NOTES:
1. [X] EDGE CONNECTOR P.N. NO. OR LETTER
2. CAPACITORS .01 μf UNLESS NOTED
3. RESISTORS; VALUE IN OHMS, 1/8W, 5% UNLESS NOTED

C210, C232, C233 NOT USED.



TOLERANCES (EXCEPT AS NOTED)	TAU-TRON INC
DECIMAL	TMI-SERIES
FRACTIONAL	TITLE: MULTI CHANNEL AMP
ANGULAR	DATE / DRAWING NUMBER: TM-57204

tau-tron
inc
27 Industrial Ave., Chelmsford, MA 01824
Tel: (617) 256-9013 TWX: 710-343-6781

INSPECTION

1. MECHANICAL

If any damage is observed on the shipping carton, ask that the carrier's agent be present during unpacking. In the event that any external damage is found on the instrument, notify the carrier and Tau-Tron as soon as possible. Follow claims procedure below.

2. ELECTRICAL

Check out the electrical performance of the instrument as soon as possible after receipt. Should any malfunctions be observed, follow the claims procedure below.

3. CLAIMS

If the unit has mechanical damage or fails electrical check-out, notify Tau-Tron immediately. For mechanical damage which occurred during shipment, notify the carrier also. The Tau-Tron Customer Service Department will arrange for repair or replacement of the instrument. A Return Authorization number will be issued for all returns.

4. REPACKAGING

Use the original shipping carton and materials, if available. Otherwise use a double-walled carton (test strength of 350 pounds), and shock absorbing material such as bubble-wrap to prevent instrument from moving in the shipping carton during transit. Secure package by sealing with heavy paper tape.

27 Industrial Avenue, Chelmsford, MA 01824 (617) 256-9013